APPLICATION FOR
UNITED STATES PATENT

in the name of

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For

SPLIT-CHANNEL HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) DEVICE

TECHNICAL FIELD

[0001] This invention relates to high electron mobility transistor (HEMT) devices, and more particularly to HEMT devices having split-channels.

BACKGROUND

[0002] As is known in the art, one type of semiconductor device is a High Electron Mobility Transistor (HEMT). One type of HEMT is a metamorphic HEMT (MHEMT) such as that shown in the cross-section in FIG 1. The device is constructed by growing crystal compounds containing In, Ga, Al, and As on GaAs wafers. In these devices, electrons are conducted into and out of the device's semiconductor layers by means of ohmic metal contacts. Upon entering the semiconductor layers below the source ohmic metal, electrons are routed to a channel layer consisting of InGaAs. Once in the channel layer, electrons are confined there by virtue of an InAlAs Schottky layer and an InAlAs barrier layer until they again reach the drain ohmic contact. Electrons have an affinity for the channel layer because the electronic properties of the InGaAs and InAlAs are such that electrons are at a lower potential energy when they reside in the InGaAs channel layer. InGaAs cap layers combined with a high-temperature bake, i.e. alloy of the ohmic metal, serve to aid the formation of low-resistance ohmic contacts which aid the entry and exit of electrons to and from the channel layer.

[0003] Devices similar to the MHEMT in form and function can also be constructed on InP substrates. The resulting InP HEMTs have similar electrical properties to MHEMTs but are more restricted in terms of material composition design.

[0004] As is also known in the art, MHEMTs and similar devices are typically used to amplify electrical signals at frequencies up to approximately 150 GHz. Present challenges include obtaining high efficiency, power, and gain above 60 GHz along with low cost, and design flexibility that allows trade-offs to be made between power density and gain. In order to reduce cost, these devices utilize metamorphic growth technology described in a paper entitled "Molecular beam epitaxial growth and device performance of metamorphic high electron mobility transistor structures fabricated on GaAs substrates' by W. E. Hoke, P. J. Lemonias, J. J. Mosca, P. S. Lyman, A. Torabi, P. F.

Marsh, R. A. McTaggart, S. M. Lardizabal, and K. Hetzler, published in the Journal of Vacuum Science and Technology B **17**, 1131 (1999). This process allows the fabrication of high indium content channel layers as needed to obtain acceptably high gain above 60GHz.

[0005] Normally, InP substrates must be used to grow devices having channel layers with indium contents near 45-60% as required for acceptable frequency response at mm-wave frequencies. However, the metamorphic growth technology allows the growth of such high indium devices on GaAs substrates, thus reducing wafer breakage and improving manufacturability. Additionally, metamorphic technology allows one to vary the channel indium content upward, for low-power applications, to obtain low noise and high gain at high frequencies or downward to obtain higher power output while sacrificing noise figure as would be done for power amplifier applications.

[0006] Power-added efficiency (PAE), is defined

as: $PAE = \dfrac{P_{RFout} - P_{RFin}}{P_{DC}} = P_{RFout}\dfrac{(1-\dfrac{1}{G})}{P_{DC}}$ where P_{DC} is the DC power drawn by the

amplifier, P_{RFout} and P_{RFin} are the amplifier RF output and RF input signal powers

respectively, and $G = \dfrac{P_{RFout}}{P_{RFin}}$ is the amplifier power gain. Alternatively, PAE can be

defined as: $PAE = \dfrac{\delta(G-1)}{G}$ where the drain efficiency δ is defined as: $\delta = \dfrac{P_{RFout}}{P_{DC}}$. In

order to maximize PAE, it is important to maintain a high gain, well over unity. PAE is typically quoted as a percentage obtained by multiplying the above PAE by 100.

[0007] FIG 2 shows an RF load line (11) overlaying the MHEMT's family of IV

curves and the RF power output can be found from: $P_{RFout} = \dfrac{(V_{max} - V_{min})(I_{peak} - I_{min})}{8}$.

The RF voltage swing, $V_{max} - V_{min}$ and current swing, $I_{peak} - I_{min}$ are limited by the MHEMT's family of curves. Limitations on any of the four V_{max}, I_{min}, V_{min}, and/or I_{peak} will limit RF power output. V_{min} and I_{peak} are constrained to $V_{min} > 0$ and $I_{peak} < I_{dpeak}$ as shown in FIG. 2, by the device's on resistance, R_{on}. In MHEMTs, V_{max} is usually limited by the requirement to set the drain RF load and/or the DC drain bias voltage so that V_{ds}

always remains below that which induces a fast, destructive burnout process. It appears that this burnout mechanism is related to the rate of impact ionization in the channel which is proportional to I_{ds} as well as V_{ds}. Therefore the value of V_{ds} resulting in burnout, i.e. V_{burn}, generally falls as I_{ds} increases. Additionally, depending on the device, I_{min} can sometimes be nonzero due to the inability to pinch off the MHEMT drain current, I_{ds} at a high drain voltage V_{ds}. However, for devices containing high channel indium contents such as MHEMTs discussed here, the above burnout mechanism is usually the limiting factor of V_{max}.

[0008] Technology limitations in ohmic contacts as well as trade-offs inherent in doping dictate a minimum practical value of R_{on}. A nonzero R_{on} limits the drain efficiency δ because it reduces the RF current and voltage swing, and hence P_{RFout} without a proportional reduction in P_{DC}. Once the ohmic contacts are optimized, the only way left to further improve δ is to increase the value of V_{burn} by reducing impact ionization. For a given V_{ds} and device structure, impact ionization can be reduced by increasing the bandgap of the material by reducing the channel layer indium content.

[0009] Established PHEMT technologies use approximately 19% indium content in the channel and give approximately 2dB gain at maximum P_{RFout} at 95GHz whereas a 53% indium channel MHEMT has shown 5dB gain at 95 GHz at maximum P_{RFout}. Gain is a significant factor in PAE. For example, if the PHEMT and MHEMT had the same drain efficiency δ, then the MHEMT's PAE would twice that of the PHEMT. For instance, at the low gains encountered in 95 GHz PHEMTs, PAE is 0.37δ whereas the MHEMT's PAE is 0.68δ. Furthermore , PHEMT amplifiers show typically 95GHz PAEs in the range of 13% whereas InP and MHEMT PAEs are 20-24% at 95GHz. Therefore, it is important to find a device structure that will allow a good compromise between low impact ionization and high gain at high frequencies.

[0010] As is also known in the art, conventional InP and metamorphic HEMTs (MHEMTs) use a single channel layer as shown in FIG 1. Here, electrons flow in a homogenous sheet, i.e. the channel layer which has a uniform composition. While such devices obtain record low noise figures at high frequencies, the high indium content of their channel layers results in power limitations such as high gate current and low burnout voltage threshold (V_{burn}) due to the high levels of impact ionization at high values of

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drain voltage, V_{ds}. The solution might appear to be one of simply lowering the indium content of the channel. However, reduced indium content will decrease electron mobility and electron velocity. The result will be reduced gain and efficiency at high frequencies.

[0011] As is also known in the art, compromises are possible whereby the indium content is decreased to 40-50% from the 60% channel indium content as used in MHEMTs designed for low noise and small signal applications. One technique used to provide a compromise involves splitting the channel layer into upper and lower channel layer as shown in FIG. 3. In most cases, the upper channel layer consists of $In_xGa_{1-x}As$ where $0.53<x<0.65$ and the lower channel layer is InP. In some cases a portion of the InP channel is doped. Here, the high electron mobility characteristics of the upper channel enables excellent ohmic contacts and high electron velocity in the low electric field region, between gate and source, as shown in FIG. 3. Below the upper channel layer the lower InP channel layer is optimized for high electron velocity transport for high electric fields. In the low field region, the upper channel layer's greater electron affinity confines most of the current in the upper channel layer. In the high field region between the gate and drain , the electrons attain high energies and velocity due to the high electric field. While the material of the upper channel layer allows electrons to obtain high velocity at low electric fields, at high electric fields, the high scattering rate of electrons will cause their velocity to level off or drop in the upper channel. This causes the current path to shift more into the InP in the high field region where the electrons can attain reduced scattering and greater velocity under the high E-field conditions of high field region. InP also offers the benefit of reduced impact ionization relative to InGaAs. The net result is with InP in the lower channel layer the device should obtain a higher net electron velocity giving it improved high-frequency gain. The reduced impact ionization of the lower channel layer will allow such a device to operate at higher V_{ds} and allow higher RF output power than could be obtained with an all $In_xGa_{1-x}As$ with $0.53<x<0.60$.

[0012] While making the lower channel from InP appears to be attractive, it presents the problem of growing phosphorus-containing materials which can be difficult in the molecular beam epitaxy (MBE) systems often used for device layer growth. Furthermore, growth of As-containing materials such as the InGaAs upper channel layer on an InP lower channel layer can be complicated because of material quality difficulties

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transitioning from InP to InGaAs growth. Growth on InP substrates introduces the need for enhanced care to prevent breakage, requires unique via processing relative to GaAs, and allows only a limited variation of indium content in the channel. InP in the device channel can require a redesign of the ohmic metals which had proven reliability and low resistance for all-InGaAs channel devices. Finally, the presence of InP, in the devices' active layers requires special etchants, which complicates the isolation mesa etch process step because InP requires a different etchant than the rest of the As-based materials.

SUMMARY

[0013] In accordance with the present invention, a transistor structure is provided having a semiconductor substrate; a barrier layer disposed over the substrate; a lower channel layer disposed on the barrier layer; an upper channel layer disposed on the lower channel layer, such lower channel being of the same material as the upper channel, the upper and lower channels having different mole fractions of an common element used in such upper and lower channel layers; and an Schottky layer on the upper channel layer.

[0014] In one embodiment, the lower channel layer has a bandgap greater that the bandgap of the upper channel layer.

[0015] In one embodiment, the lower channel layer has a bulk electron mobility lower than the bulk electron mobility of the upper channel layer.

[0016] In one embodiment, the substrate comprises GaAs and wherein the upper and lower channel layers comprise InGaAs.

[0017] In one embodiment, the upper and lower channel layers include indium.

[0018] In accordance with another feature of the invention, a transistor structure is provided. The structure includes a gallium arsenide (GaAs) semiconductor substrate; an indium aluminum gallium arsenide lattice match layer; an indium aluminum arsenide (InAlAs) barrier layer disposed over the lattice-match layer; an $In_y Ga_{1-y}$ As lower channel layer disposed on the barrier layer, where y is the mole fraction of In content in the lower channel layer; an $In_x Ga_{1-x}$ As upper channel layer disposed on the lower channel layer, where x is the mole fraction of indium content in the upper channel layer and where x is different from y; and an InAlAs Schottky layer on the $In_x Ga_{1-x}$ As upper channel layer.

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[0019] In one embodiment, the lower channel layer has a bandgap greater that the bandgap of the upper channel layer.

[0020] In one embodiment, the lower channel layer has an electron mobility lower than the electron mobility of the upper channel layer.

[0021] In one embodiment, x is in the range between 0.15 and 0.90 and y is in the range between 0.0 and 0.65.

[0022] In one embodiment, x is substantially 0.53 and y is substantially 0.43

[0023] Such transistor structure has most of the benefits of the InP split-channel HEMT but uses a GaAs substrate and has a phosphorus-free layer structure. The structure enables the use of indium contents outside the normal range allowed on InP substrates and allows a greater range of indium content relative to devices grown on InP substrates. The split channel (i.e., upper and lower channel layers of the present invention) allows independent optimization of the upper channel layer for excellent electron transport at the low electric field conditions found in the low electric field region between gate and source while performing an independent optimization on the lower channel layer material to obtain optimum electron transport while minimizing impact ionization in regions having a high electric field such as between the gate and drain.

[0024] Thus, the device achieves an excellent compromise between these two opposing parameters (i.e., low impact ionization and high gain at high frequencies) while enjoying the low cost and manufacturability afforded by the use of GaAs substrates.

[0025] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0026] FIG. 1 is a single-channel cross-sectional; sketch of a metamorphic HEMT device according to the PRIOR ART;

[0027] FIG. 2 is a plot showing a family of current-voltage (IV) curves for the device of FIG. 1 according to the PRIOR ART;

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[0028] FIG. 3 is a split-channel cross-sectional; sketch of an InP composite-channel HEMT device according to the PRIOR ART;

[0029] FIG. 4 is a cross-sectional; sketch of a split-channel HEMT device according to the invention; FIGs. 5 and 6, respectively, are a comparison of IV curves (left plot) and on-state breakdown curves (right plot) the device of FIG. 1 according to the PRIOR ART with the device of FIG. 4 according to the invention;

[0030] FIG. 7 is the breakdown data of FIGS. 5 and 6 in a more compact format;

[0031] FIG. 8 are frequency response curves of the device of FIG. 1 according to the PRIOR ART and devices FIG. 4 according to the invention;

[0032] FIG. 9 are the differences between maximum available gain (MAG) and current gain (H21) of the invention and the device of FIG 1 (prior art) measured and Vds = 2.5V and 1.5V.

[0033] FIG. 10 shows P_{RFout}, PAE, and associated gain (G) curves as a function of the input RF drive power (P_{RFin}) for the device of FIG. 4 according to the invention.

[0034] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0035] Referring now to FIG. 4 an MHEMT device structure 10 is shown to include a GaAs semiconductor substrate 12, an InAlAs barrier layer 14, and lattice matching layers 16 between the barrier layer 14 and the substrate 12. Here, the barrier layer 14 is 1000 Angstroms thick.

[0036] Disposed on the barrier layer 14 is an $In_y Ga_{1-y}$ As lower channel layer 18, where y is the mole fraction of In content in the lower channel layer, where y is in the range of 0.0 to 0.65, here 0.43. Here, the lower channel layer 18 is 100 Angstroms thick.

[0037] Disposed on the lower channel layer 18 is an $In_x Ga_{1-x}$ As upper channel layer 20, here 100 Angstroms thick, where x is the x is the mole fraction of In content in the upper channel layer and where x is in the range of 0.15 to 0.90, here 0.53 It is noted that x is different from y.

[0038] Disposed on the upper channel layer 20 is a Schottky layer 22. The Schottky layer 22 is here 180 Angstroms thick, it being noted that there is a conventional

silicon doping spike 24, here 40 Angstroms from the bottom of the Schottky layer 22, as indicated. The bottom 40 Å of the Schottky layer 22 is composed of $In_{0.52}Al_{0.48}As$ while the top 140 Å of the Schottky layer 22 is composed of $In_{0.4}Al_{0.6}As$.

[0039] The device structure 10 includes InGaAs cap layers 26a and 26b, here 70 Angstroms thick and silicon doped to $5x10^{18}/cm^3$. A gate electrode 28 is in Schottky contact with the Schottky contact layer 22 in a region between the cap layers 26a, 26b. The region has a low field region and a high field region, as indicated. A source electrode 30 is in ohmic contact with the cap layer 26a and a drain electrode 32 is in ohmic contact with cap layer 26b, as indicated. Doping in the cap layers 26a and 26b as well as the doping spike 24 represents the total of the intentional doping of the device.

[0040] Dotted arrow 34 represents the path of electron flow between the source and drain electrodes 30, 32 through the upper and lower channel layers 20, 18.

[0041] It is noted that the structure uses an GaAs substrate and is phosphorus-free. The resulting device is thereby known as the split-channel metamorphic HEMT (split-channel MHEMT). MHEMT technology allows a greater range of indium content relative to devices grown on InP substrates. The split channel allows independent optimization of the upper channel for excellent electron transport at the low electric field conditions found in the low field region while allowing an independent optimization on the lower channel material to obtain optimum electron transport in regions having a high electric field such as between the gate 28 and InGaAs cap layer 26b. The upper channel layer 20 as noted above contains $In_xGa_{1-x}As$ where x and y are the mole fractions of the indium contents for the respective channels. In the implementation here, the upper channel layer 20 has an indium mole fraction set to x = 0.53 while the lower channel layer 18 has y = 0.43. This arrangement gives the following calculated material parameters:

Table 1

Calculated electrical characteristics of MHEMT channel materials

	Indium mole fraction	Bandgap (eV)	Bulk Mobility
Upper channel	0.53	0.74	9760

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layer 20			
lower channel layer 18	0.43	0.85	8700

[0042] The larger bandgap of the lower channel layer 18 should reduce impact ionization and hence raise the value of V_{ds} that the MHEMT can reliably withstand. In the low-field region, electron velocity is enhanced by the higher mobility of the upper channel whereas in the high-field region, the reduced impact ionization of the lower channel layer 18 allows higher V_{ds}. Electrons are confined in the two channel layers 18, 20 due to the potential barriers formed by the Schottky layer 22 and barrier layer 14 materials. This confinement combined with the small 200Å combined width of the channel layers 18, 20 results in the electrons' residing at discrete energy levels. Quantum mechanical simulations show that the conduction band of upper channel is 0.1eV lower in energy than that of the lower channel - indicative of the upper channel layer's 20 higher affinity for electrons relative to the lower channel layer 18. The MHEMT's layer structure 10 is such that the first electron energy level is below the conduction band of the lower channel layer 18. In the low-field region, the conduction bands of the dual channel layer 18, 20 tend to therefore skew the electron distribution toward the upper channel layer 20 and hence, in the low-field region the electronic transport is dominated by the characteristics of the higher indium upper channel layer 20. However, in the high-field region, one can expect the electrons to fill the upper energy levels. These excited electron energy levels e.g. the second and higher energy levels, exceed the 0.1 eV difference in conduction band levels between the upper and lower channel layers 18, 20. Therefore, energetic electrons are able to readily cross to the lower channel layer 18, where they are less likely to contribute to impact ionization and device burnout.

[0043] The split-channel MHEMT devices 10 are constructed via the following procedure:

[0044] All semiconductor layers are grown using an molecular beam epitaxy system (MBE). First the metamorphic lattice-matching layers 16 are grown on an Epi-ready GaAs wafer (i.e., substrate 12) as described in the article referred to above. For the split-channel MHEMT device 10, the lattice-matching layer 16 begins with a layer of

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InAlGaAs with a 0.05 mole fraction of indium. The indium content is increased with subsequent InAlGaAs layers while the gallium layer mole fraction is decreased and the aluminum mole fraction held constant. After 4500Å of these layers, the InAlAs is grown and the In is ramped up in concentration while the Al is ramped down for the next 6000Å of growth. The lattice match layer technology is also discussed in the paper "Strain Relaxation and Dislocation Filtering in Metamorphic High Electron Mobility Transistor Structures Grown on GaAs Substrates" D. Lubyshev, W. Liu, T. Stewart, A. Cornfeld, X. Fang, X. Xu, P. Specht, C. Kisielowski, M. Naidenkova, M. Goorsky, C. Whelan, W. Hoke, P. Marsh, J. Millunchick, S. Svensson, Journal of Vacuum Science and Technology B 19(4), July/August 2001.

[0045] Finally layers having a lattice constant close to that of the channel layers, 18 and 20 are grown starting with the lower $In_{0.52}Al_{0.48}As$ barrier layer 14.

[0046] The two channel layers (split channel), i.e., lower channel layer 18 and upper channel layer 20, follow as shown in FIG. 4, and are covered by the 40Å lower portion of the Schottky layer 22. Here, the 40Å lower portion of the Schottky layer 22 is $In_{0.52}Al_{0.48}As$. For the upper portion of the InAlAs Schottky layer 22, the aluminum content is then raised to 0.6 fraction giving an $In_{.4}Al_{.6}As$ 140Å Schottky layer. The silicon pulse layer 24 is disposed between the upper and lower portions of the Schottky layer 22.

[0047] The Schottky layer's 22 high aluminum content in the upper portion thereof is designed to reduce gate current via the formation of a large energy barrier between gate electrode 28 and channel layers 18, 20 combined with a large Schottky barrier (ϕ_b) between Schottky layer 22 and the gate metal electrode 28.

[0048] After growth of layers, the split-channel MHEMT devices are defined and electrically isolated by performing a mesa etch which removes semiconductor material between the devices down to the layer 16. The ohmic contacts 30, 32 are deposited and alloyed. Next, the gate region is defined and etched to form the region between the layers 26a and 26b using E-beam and optical lithography. The gate electrode 28 metal is then deposited and lifted off to form the gate electrode 28..

[0049] It is noted that two channels layer 18 and 20 are provided, i.e., the lower channel $In_yGa_{1-y}As$ layer 18 and the upper channel $In_xGa_{1-x}As$ layer 20 where x and y are

the mole fractions of the channels' indium contents and x>y. Further, it is noted that the active device semiconductor layers 18-22 have an average lattice constant different from the lattice constant of InP.

RESULTS

[0050] Several split-channel devices 10 (FIG. 4) and single-channel MHEMTs according to FIG. 1 having gate lengths, L_g, of 0.15µm and a gate periphery of 100µm were probed on-chip using a 50Ω wafer probe system. The split-channel MHEMTs devices 10 (FIG. 4) had a 100Å thick upper channel layer 20 of $In_{.53}Ga_{.47}As$ and a 100Å lower channel layer 18 of $In_{.43}Ga_{.57}As$. The single-channel MHEMT had a 200Å thick $In_{.53}Ga_{.47}As$ channel. Hereafter the above MHEMT designs are referred to as 43/53% and 53% In MHEMTs. Other MHEMTs were tested which were similar to those of FIG 1 but which had 200Å thick $In_{.6}Ga_{.4}As$ channels. These devices were referred to as 60% In MHEMTs.

[0051] In these tests, bias tees, to be described, were used only on the gate circuit. Control of impedance presented to the MHEMT, particularly the gate, is important to prevent undesirable oscillation. The bias tees serve this purpose by isolating the DC and RF signal paths so that the RF signal path on the gate sees 50Ω loads while the DC gate bias voltage is applied to the device's gate and blocked from the RF 50Ω load.

[0052] Hereafter, all MHEMT current will be listed as normalized to the total gate periphery of one mm e.g. 10mA/mm means a current of 10mA for each mm of gate periphery where periphery is the dimension of the gate perpendicular to the current flow and is a measure of device size.

[0053] The first test is to measure the MHEMTs' current-voltage family of curves, hereafter known as the IV curves, via an HP4155B parameter analyzer. In this test, the drain current, I_{ds}, is plotted as a function of both drain-source voltage, V_{ds}, and gate-source voltage, V_{gs}. A family of I_{ds} vs. V_{ds} curves is generated by setting V_{gs}, sweeping V_{ds} from 0 to 1.5 V and plotting the resulting I_{ds} with V_{gs} held constant. Subsequent curves are generated by stepping V_{gs} by -0.2 V and sweeping V_{ds} to generate the next of a series of curves. This process is repeated from V_{gs} = +1V to V_{gs} of −1.1 or − 1.2V. Since gate current is limited to 100µA/mm, the actual V_{gs} will limit somewhere below +1V.

[0054] Breakdown and burnout measurements have been used here to evaluate and compare the power output capabilities of three types of MHEMT structures; namely a 53% MHEMT having a 200Å thick $In_{.53}Ga_{.47}As$ channel, (as shown in FIG. 1) and a 43/53% MHEMT being a split-channel MHEMT device 10 as in FIG. 4, having an upper 100Å thick channel layer 20 of $In_{.53}Ga_{.47}As$ and a 100Å thick lower channel layer 18 of $In_{.43}Ga_{.57}As$. The 53% and 43/53% MHEMTs devices 10 (FIG. 4) are competing MHEMT designs intended for RF power production above 60GHz. For comparison, some of the tests included data from MHEMTs similar to the 53% devices but having $In_{.6}Ga_{.4}As$ channels and referred to below as 60% MHEMTs.

[0055] On-state breakdown characteristics can be measured after an MHEMT's operation has been verified via the IV family of curves. On-state breakdown is measured by sweeping I_{ds} from zero to 300mA/mm by plotting a family of I_{ds} vs. V_{ds} curves . Each curve is plotted at a unique value of reverse gate current, I_g; and each different curve of the family is produced by stepping I_g to a new value. Gate current arises principally from two effects namely 1. tunneling and 2. hole current generated by impact ionization in the channel layer. For a given value of V_{gs}, I_g is expected to rise as I_{ds} and/or V_{ds} increases because the resulting increase in impact ionization increases hole generation in the channel. Holes are gathered by the gate resulting in a gate current proportional to the hole generation rate. At low I_{ds}, one would expect I_g to be dominated by electron tunneling between gate metal 28 and the channel layers 18 and 20.In FIGS. 5 and 6, respectively, 53% and 43/53% split-channel MHEMTs were characterized by plotting their IV curves (left plot) and then their on-state breakdown curves (right plot). For the 53% data, IV and breakdown curves were averaged from four MHEMTs. In FIG. 6, the 43/53% IV curves were averaged for four MHEMTs and their breakdown curves represent averages over two devices. One will notice that while the 53% devices show higher breakdown V_{ds} at low drain currents, for $I_{ds} > 100$mA/mm, the 43/53% devices show an advantage with V_{ds} higher than that of the 53% MHEMTs for a given gate current I_g.

[0056] FIG. 7 illustrates some of the breakdown data of FIGS. 5 and 6 in a more compact format. In all cases, each data point represents V_{ds} at I_g=200µA/mm for a single device. The V_{ds} value, at each data point, was formed by the average of two V_{ds} values measured at two respective I_{ds} values of 200 and 300mA/mm with I_g=200µA/mm in all

cases. In FIG. 7, the "post SiNx" devices were 43/53% MHEMTs which had been passivated with a silicon nitride coating The 60% In devices, had also been passivationed with a silicon nitride coating while the 53% devices were measured before passivation. FIG. 7 illustrates the expected trends, namely that the split-channel 43/53% MHEMTs show higher on-state breakdown, i.e. higher V_{ds}, than the 53% In MHEMTs. Another trend is seen as well, namely that as I_{max} increases V_{ds} at breakdown decreases. This is expected because I_{max} is the maximum value of I_{ds} obtainable in the devices and it is related to the doping. A higher Si pulse doping 24 (FIG. 4) is expected in increase gate reverse current by reducing the effective energy barrier to electrons presented by the Schottky layer 22. Also, higher doping and I_{max} levels act to reduce the gate-drain depletion region width which increases the high field region's electric field for a constant V_{ds}. The higher electric field increases impact ionization in the channel regions, i.e., either the single channel layer for the device shown in FIG. 1 or the split channel layer 18, 20 for the device 10 in FIG. 4, while reducing the barrier to gate current flow. These effects lead to a higher gate current for a given V_{ds} or alternatively a lower V_{ds} for a given drain and gate current.

[0057] Hall measurements of the semiconductor layer structures of the 53% (FIG. 1) and 43/53% (i.e., device 10 in FIG. 4) MHEMTs show measured room-temperature Hall mobilities of 9624 and 9097cm^2/V•S respectively. FIGS. 8 and 9 show the small-signal frequency response of the 43/53% split-channel vs. that of the 53% MHEMTs. At 95GHz and Vds=2.5V, FIG. 8 shows both devices having a small-signal maximum available power gain (MAG) of 11.6dB. At 95GHz the 53% MHEMT has an H_{21} of 5.6dB while that of the 43/53% MHEMT is 6.2dB. At a V_{ds} of 2.5V and I_{ds} of 200mA/mm the current gain, H_{21}, of the 43/53% device is 0.6-0.8dB higher than that for the 53% device while MAG values are nearly identical for both devices from 10-100GHz.

[0058] FIG. 9 shows the effect of increasing V_{ds} on a comparison of the 43/53% vs. 53% devices. For a V_{ds} of 1.5V, H_{21} of the 43/53% MHEMT exceeds that of the 53% MHEMT by 0.65dB at 10GHz and 0.3dB at 100GHz. Here the MAG of the 43/53% device is ~0.05dB less than that of the 53% MHEMT. FIG. 9 shows the measured differences between maximum available gain (MAG) and current gain (H_{21}) of the

invention compared against that of prior art and V_{ds} = 2.5V and 1.5V. For example the curve labeled "2.5V H_{21}" represents the H_{21} (in dB) of the invention minus the H_{21} of the prior art with both devices' H_{21} values measured at V_{ds} = 2.5V. Similarly, "1.5V MAG" is the invention device MAG minus that of the prior art device with both measured at V_{ds} = 1.5V.

[0059] It is noted that, as V_{ds} increases to 2.5V, the difference in MAG values goes to nearly zero while the difference in H_{21} increases by about 0.2dB across the 10-100GHz band. In other words, as V_{ds} increases the 43/53% MHEMT's advantage in gain increases in terms of both H_{21} and MAG. This is to be expected because, compared to the 53% MHEMT, as V_{ds} increases, impact ionization electron scattering in the channel increases less rapidly in the 43/53% MHEMT giving this MHEMT an increasing advantage in electron mobility, over the 53% MHEMT, as V_{ds} is increased. While the 43/53% MHEMT's frequency response advantage is minor, it does achieve the desired improvement in on-state breakdown, as defined in an article entitled "Breakdown in Millimeter-Wave Power InP HEMTs: a Comparison with PHEMTs" by J. del Alamo and M. Somerville, published in IEEE Journal of Solid-State Circuits, Vol. 34, No. 9, September 1999, pp 1204-1211, without a penalty in frequency response relative to the 53% MHEMTs.

[0060] FIG. 10 shows P_{RFout}, PAE, and associated gain (G) as a function of the input RF drive power (P_{RFin}) at 95GHz. At the maximum PAE of 23%, P_{RFout} is 13.8dBm=24mW or about 160mW/mm with an associated gain of approximately 6dB. The input RF power was set to 3dB compression i.e. a level that reduced the gain by 3dB relative to that with a small RF input. The 23% PAE is near state of art efficiency for any InP HEMT or MHEMT operating at or near 95GHz. A device's gain is the ratio of output RF signal power delivered to a load resistor on the output of the device divided by the RF signal power delivered to the device's input.

[0061] A device's maximum available gain (MAG) is the maximum gain theoretically available from the device when the device is presented with optimum impedances at the input and output.

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[0062] As shown here, H_{21}, is the magnitude of device's current gain, i.e. the ratio of the device's output signal current divided by its input signal current with the output tied to ground (set to 0V).

[0063] A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.

What is claimed is: